WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a substrate having a lattice structure and having an implanted precipitate region located within said lattice structure;

a dynamic defect located within said lattice structure and proximate said implanted precipitate region, such that said implanted precipitate region affects a position of said dynamic defect within said lattice structure; and

a gate structure located over said substrate.

2. The semiconductor device as recited in Claim 1 wherein said implanted precipitate region comprises a SiO_2 precipitate region.

3. The semiconductor device as recited in Claim 1 wherein said implanted precipitate region comprises a SiN precipitate region.

4. The semiconductor device as recited in Claim 1 wherein said implanted precipitate region is located from about 60 nm to about 150 nm below said gate structure.

5. The semiconductor device as recited in Claim 1 wherein

said implanted precipitate region is noncontinuous.

6. The semiconductor device as recited in Claim 1 wherein said dynamic defect is an edge dislocation, a vacancy, a dislocation loop formed by an agglomeration of vacancies within said lattice, a silicon self-interstitial atom, a substitutional atom, or a dislocation loop formed by the agglomeration of self interstitial atoms.

7. The semiconductor device as recited in Claim 1 wherein said substrate is a first silicon substrate and said device further includes a silicon-germanium layer located over said first silicon substrate and a second silicon substrate located over said silicon-germanium layer, wherein said silicon-germanium layer is in a relaxed state and said second silicon substrate is in a stressed state.

8. The semiconductor device as recited in Claim 1 wherein said substrate is a first silicon substrate and said device further includes an implanted silicon-germanium region within said first silicon region and a second silicon substrate located over said first silicon substrate, wherein said second silicon substrate is in a stressed state.

9. The semiconductor device as recited in Claim 1 wherein said substrate is a first silicon substrate and said device further includes a silicon or germanium implant induced dynamic defect region within said first silicon region wherein said first silicon substrate is in a stressed state induced by said silicon or germanium implant induced dynamic defect region.

10. A method for forming a semiconductor device, comprising:

providing a substrate having a lattice structure;

implanting a precipitate region within said lattice structure;

introducing a dynamic defect within said lattice structure and proximate said implanted precipitate region, such that said implanted precipitate region affects a position of said dynamic defect within said lattice structure; and

forming a gate structure over said substrate.

11. The method as recited in Claim 10 wherein said implanting includes implanting a SiO_2 precipitate region.

12. The method as recited in Claim 10 wherein said implanting includes implanting a SiN precipitate region.

13. The method as recited in Claim 10 wherein said precipitate region is located from about 60 nm to about 150 nm below said gate structure.

14. The method as recited in Claim 10 wherein said precipitate region is noncontinuous.

15. The method as recited in Claim 10 wherein said dynamic defect is an edge dislocation, a vacancy, a dislocation loop formed

by an agglomeration of vacancies within said lattice, a silicon self-interstitial atom, a substitutional atom, or a dislocation loop formed by the agglomeration of self interstitial atoms.

16. The method as recited in Claim 10 wherein said substrate is a first silicon substrate and said method further includes forming a silicon-germanium layer over said first silicon substrate and forming a second silicon substrate over said silicon-germanium layer, such that said silicon-germanium layer is in a relaxed state and said second silicon substrate is in a stressed state.

17. The method as recited in Claim 10 wherein said substrate is a first silicon substrate and said method further includes implanting silicon-germanium region into said first silicon region and forming a second silicon substrate located over said first silicon substrate, such that said second silicon substrate is in a stressed state.

18. The method as recited in Claim 10 wherein said substrate is a first silicon substrate and said device further includes a silicon or germanium implant induced dynamic defect region within said first silicon region wherein said first silicon substrate is in a stressed state induced by said silicon or germanium implant induced dynamic defect region.

19. The method as recited in Claim 10 wherein said implanting includes implanting to a peak concentration ranging from about 5E17 atoms/cm^3 to about 5E18 atoms/cm^3.

20. The method as recited in Claim 10 wherein said implanting includes implanting using an energy ranging from about 40 keV to about 70 keV.

21. The method as recited in Claim 10 further including annealing said implanted precipitate region using a temperature ranging from about 500°C to about to about 1200°C after said implanting.

22. The method as recited in Claim 21 wherein said annealing includes a first anneal at a temperature ranging from about 600°C to about 800°C and a second anneal at a temperature ranging from about 1000°C to about 1100°C.

23. An integrated circuit, comprising:

a substrate having a lattice structure and having an implanted precipitate region located within said lattice structure;

a dynamic defect located within said lattice structure and proximate said implanted precipitate region, such that said implanted precipitate region affects a position of said dynamic defect within said lattice structure;

transistors located over said substrate; and

interconnects connecting said transistors to form an operational integrated circuit.

24. The integrated circuit as recited in Claim 23 wherein said implanted precipitate region comprises a SiO_2 precipitate region.

25. The integrated circuit as recited in Claim 23 wherein said implanted precipitate region comprises a SiN precipitate region.

26. The integrated circuit as recited in Claim 23 wherein said implanted precipitate region is located from about 60 nm to about 150 nm below said gate structure.

27. The integrated circuit as recited in Claim 23 wherein

said substrate is a first silicon substrate and said device further includes a silicon-germanium layer located over said first silicon substrate and a second silicon substrate located over said silicon-germanium layer, wherein said silicon-germanium layer is in a relaxed state and said second silicon substrate is in a stressed state.

28. The integrated circuit as recited in Claim 23 wherein said substrate is a first silicon substrate and said device further includes a silicon or germanium implant induced dynamic defect region within said first silicon region wherein said first silicon substrate is in a stressed state induced by said silicon or germanium implant induced dynamic defect region.